Fabrication and Characterization of Mixed-Signal Polymer-Enhanced Silicon Interposer Featuring Photodefined Coax TSVs and High-Q Inductors

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Abstract

This paper demonstrates: (a) low-loss photodefined polymer-embedded copper vias within a 10 Ω-cm resistivity silicon to yield electrical performance similar to glass interposers; (b) coaxial polymer-embedded vias with desired wideband impedance and reduced coupling; and (c) high-Q inductors attained using the photodefined polymer-enhancement technology.

I. Introduction

The migration to multicore microprocessors has created an incredible demand for low-energy high-bandwidth off-chip communication [1, 2]. Moreover, integration of heterogeneous ICs and passives is highly desirable to build compact computing and communication systems. To address these demands, silicon interposers with vertical interconnects, called through-silicon vias (TSVs), and fine-pitch metallization have been widely explored [3-7]. Silicon interposers enable high-bandwidth low-power communication between multiple ICs (or smaller dice partitioned from a large die). Moreover, silicon interposers provide the opportunity for integration of passives closer to the ICs using short interconnects; this can enable compact systems for applications such as high-speed multimedia transfer, high-speed pico-cell cellular links, and short-range wireless communications using millimeter-wave frequency bands (V-band or D-band, for example) [6-8].

However, TSVs have significant losses and coupling at higher frequencies and frequency-dependent impedance variations [9]. Moreover, attaining high-performance passives in silicon interposers is challenging due to the frequency-dependent losses caused by the silicon substrate [6, 7]. To address these challenges, various TSV solutions including the implementation of air or polymer liners and coaxial TSVs have been demonstrated in the literature [10-12]. However, the fabrication of such TSV solutions is challenging. Alternate substrates, such as high-resistivity silicon, glass, and organic substrates, and silicon substrates with dielectric-filled wells supporting passives have been explored as possible solutions to these challenges [6, 7, 13-15]. However, high-resistivity silicon is relatively expensive, the fabrication of vias in glass is challenging, attaining high-density wiring over organic substrates is difficult, and the approaches with dielectric-filled wells in silicon require specialized processing for each passive component in addition to TSVs. These challenges necessitate the development of advanced silicon interposer technologies.

To address TSV losses and frequency-dependent impedance variations as well as performance degradation of RF passives over silicon interposers, this paper demonstrates high-performance interconnect and passive technologies for a large-area 'thick' silicon interposer that include: (a) photodefined polymer-embedded copper vias within a 10 Ω-cm resistivity silicon yielding performance similar to glass interposers [16, 17]; (b) polymer-enhanced coaxial vias with desired impedance and reduced coupling; and (c) polymer-enhanced high-Q inductors using the photodefined polymer-enhanced silicon interposer technology. Figure 1 shows an envisioned mixed-signal system using the proposed interconnect and passive technologies.

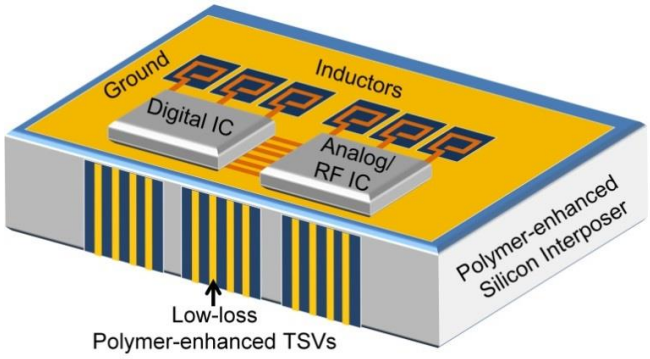
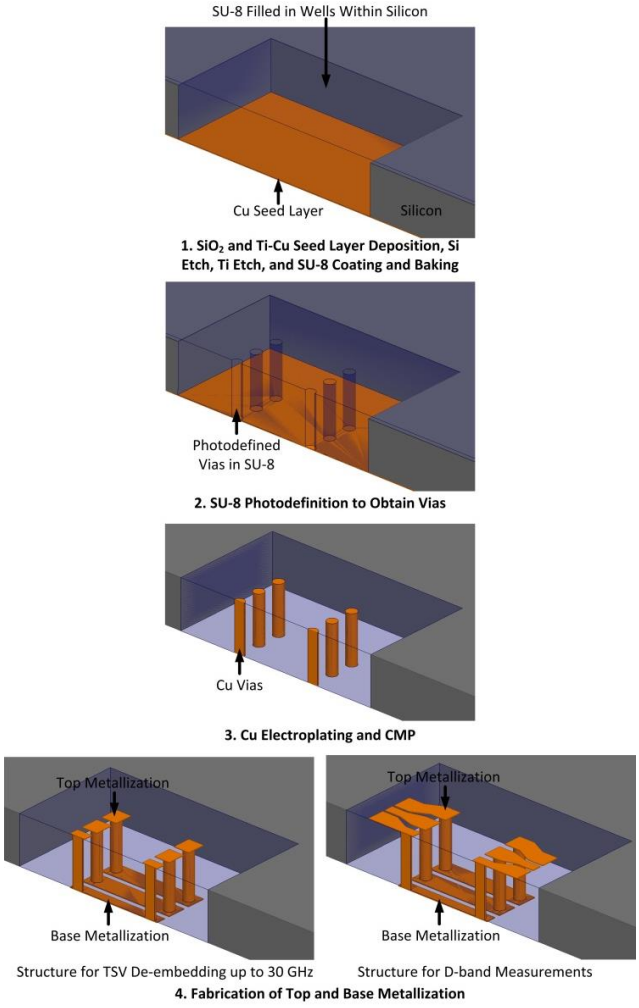


Figure 1. Envisioned mixed-signal silicon interposer module featuring polymer-enhanced TSVs and inductors.

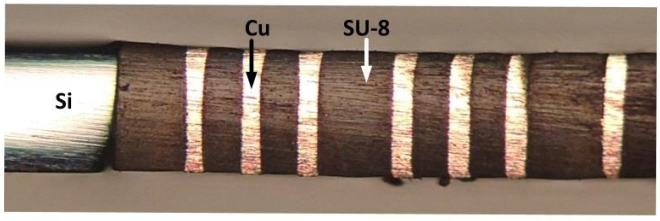
II. Polymer-embedded Vias: Fabrication, De-embedding and D-band Characterization

To begin the fabrication of polymer-embedded vias, silicon dioxide and a titanium-copper seed layer are deposited at the base of a silicon wafer followed by etching of wells using the Bosch process. Next, the silicon dioxide and titanium layers at the base are etched followed by SU-8 [18, 19] coating and photodefinition to obtain vias in the polymer-filled wells [20]. Once the vias are obtained, copper electroplating is performed followed by chemical-mechanical polishing (CMP) to remove additional copper at the top of the electroplated vias and the seed layer at the base. Next, metallization is fabricated above and below the copper vias; to facilitate de-embedding measurements of the polymer-embedded vias, pads are fabricated over the vias enabling probing close to the vias, and to perform D-band characterization, longer traces with fan-in are fabricated enabling high-frequency measurements using finer-pitch probes, as shown in Figure 2.

Figure 2 and 3 illustrate the fabricated copper vias on a 150 µm pitch within 1800 µm x 1800 µm wells. The fabricated TSV structures for de-embedding are 285 µm tall and 60 µm in diameter, and the fabricated structures for D-band characterization are 325 µm tall and 70 µm in diameter.



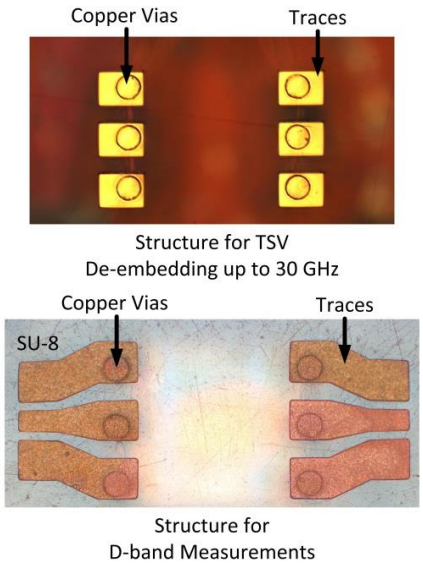
(a) Fabrication process of polymer-embedded vias.



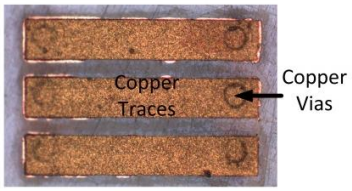
(b) Cross-section image of fabricated polymer-embedded vias.

Figure 2. Fabrication steps and cross-section of fabricated polymer-embedded vias.

To de-embed the loss of the fabricated (GSG) polymer-embedded vias, high-frequency measurements were performed up to 30 GHz. A dedicated RF probe station with a Keysight N5245A PNA-X network analyzer and Cascade Microtech 150 µm pitch |Z| Probes were used for TSV measurements, as shown in Figure 4. Moreover, for the D-band (110-170 GHz) measurements of polymer-embedded vias, a different setup including a Keysight E8361C vector network analyzer extended with an N5260A mm-wave controller and V06VNA2 mm-wave test heads were used with Cascade Microtech Infinity 75 µm pitch D-band probes. Prior to the TSV measurements, calibration of the probes was performed using the LRRM protocol. The measured results are compared to ANSYS HFSS simulations and benchmarked to simulations of TSVs with 1 µm thick silicon dioxide liner (10 Ω-cm silicon resistivity) and the same dimensions.



(a) Top view after fabrication of top metallization.



(b) Base view after fabrication of base metallization.

Figure 3. Fabricated polymer-embedded vias for de-embedding up to 30 GHz and for measurements in the D-band.

For TSV de-embedding, the L-2L technique [21] is implemented using TSV-trace-TSV structures similar to those shown in Figure 2 (with 400 µm and 800 µm long traces between the TSVs). The measured S-parameters of the two structures are converted to ABCD-parameters and the loss of the polymer-embedded vias is extracted using the L-2L technique. The de-embedding results from the measurements yield ~0.2 dB insertion loss per polymer-embedded via at 30 GHz, as shown in Figure 5. Compared to the simulated insertion loss of TSVs with silicon dioxide liners, 87% reduction in insertion loss can be obtained using the polymer-embedded vias at 30 GHz.

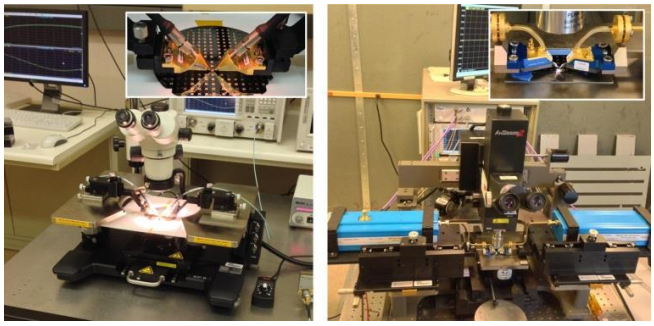


Figure 4. RF measurement setup for polymer-embedded via de-embedding up to 30 GHz (left) and for measurements in the D-band (right).

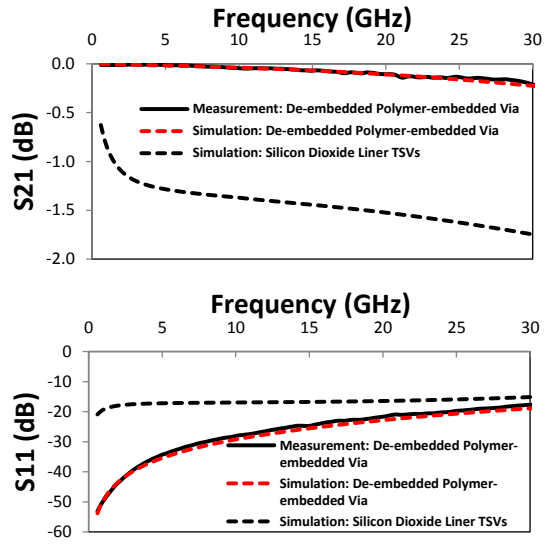


Figure 5. De-embedded polymer-embedded via loss using measurements and simulations with L-2L technique; TSVs with silicon dioxide liner included for benchmarking.

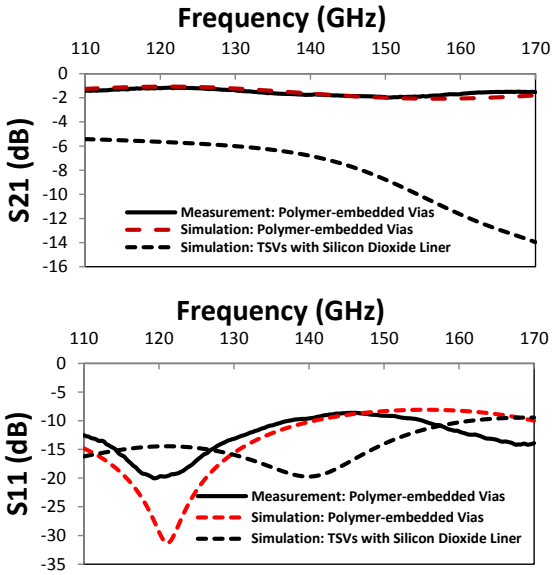


Figure 6. D-band measurements and simulations of a polymer-embedded via link; TSVs with silicon dioxide liner included for benchmarking.

Moreover, the D-band measurements of a polymer-embedded via link are demonstrated in Figure 6 showing ~1.5 dB insertion loss at 170 GHz. Compared to the simulated insertion loss of a link consisting of TSVs with silicon dioxide liner, a significant reduction in insertion loss can be obtained using the polymer-embedded vias in D-band.

III. Coaxial Vias: Fabrication and Characterization

A coaxial interconnect configuration of polymer-embedded vias is demonstrated using a fabrication process similar to the GSG configuration in the prior section, as shown in Figure 7. The fabrication of coaxial vias begins with etching of wells in a silicon wafer containing a copper seed layer at the base followed by SU-8 coating, photodefinition, via electroplating and CMP to remove overburden copper at the top of the vias. Next, top metallization is fabricated yielding coaxial vias electrically shorted at the base. Following the measurement of the short structure, the copper layer at the base is removed using CMP yielding coaxial vias that are electrically open at the base.

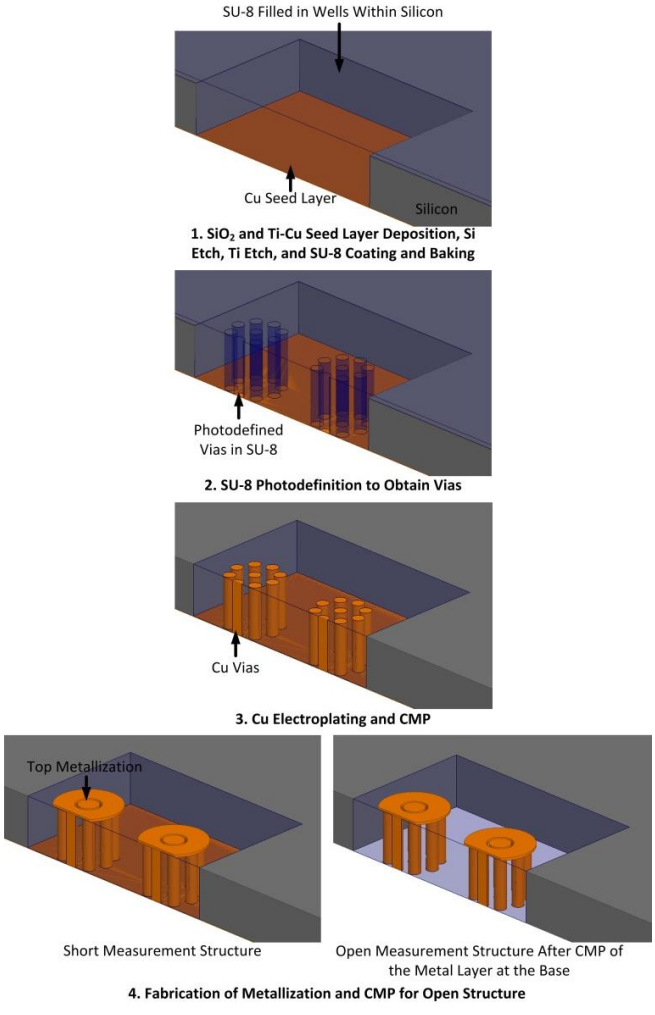


Figure 7. Fabrication process of coaxial vias.

Figure 8 illustrates the fabricated 285 µm tall polymer-enhanced coaxial vias within an 1800 µm x 1800 µm well in silicon prior to top layer metallization; the copper via

diameter is 65 µm and the signal-to-ground via pitches are 150 µm and 125 µm.

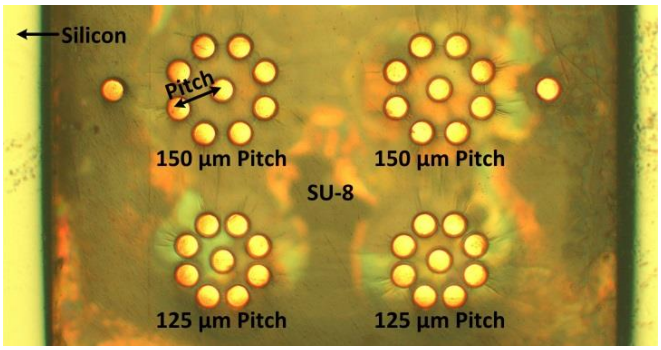


Figure 8. Fabricated coaxial vias.

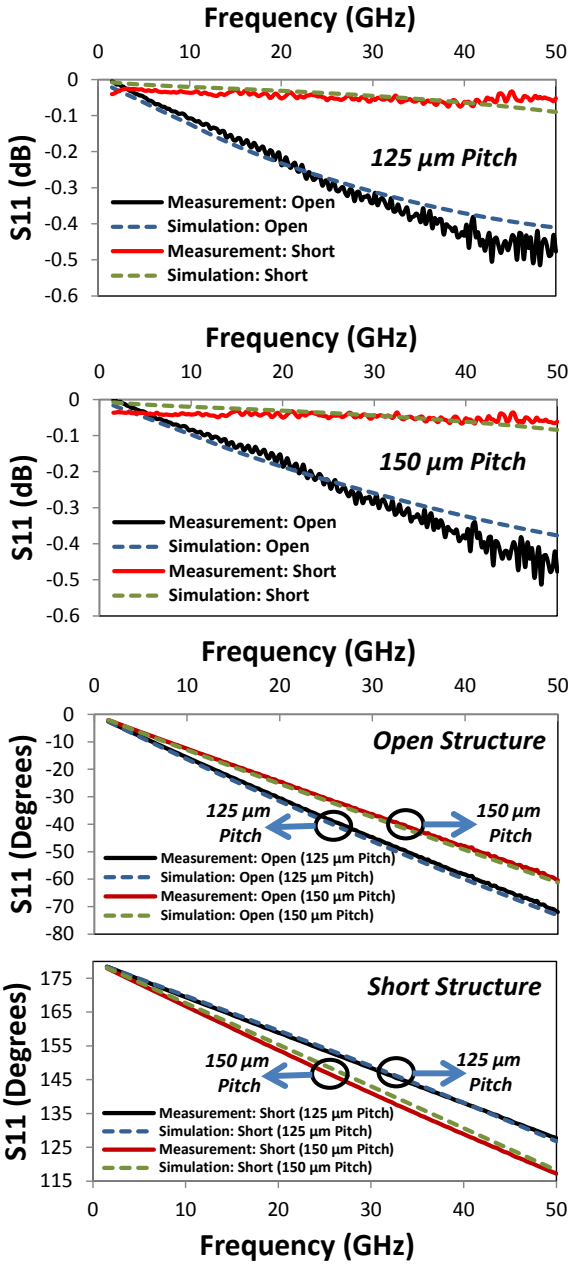


Figure 9. Single-port RF measurements of coaxial TSVs.

High-frequency measurements were performed from 1 GHz to 50 GHz for the fabricated coaxial vias, as shown in Figure 9. Using the measurements of the open structure, C and G are extracted and using the measurements of the short structure, R and L are extracted [22]. Using the measured R, L, C and G, the impedance of the fabricated coaxial vias is obtained and a wideband impedance matching is attained to approximately 50 Ω using the 150 µm pitch vias and approximately 40 Ω using the 125 µm pitch vias.

In addition to the one-port measurements, coupling measurements are also demonstrated. To fabricate the via structures for coupling measurements, following the fabrication of coaxial copper vias (Figure 7, step 3), the seed layer at the base is removed using CMP. Next, a metallization layer is formed over the fabricated vias (Figure 10) to electrically short the ground vias and perform signal-to-signal copper via coupling measurements. In the measured frequency band of 10 MHz to 50 GHz, the coaxial configuration attains an average 14.5 dB reduction in signal-to-signal via coupling compared to the non-coaxial structure, as shown in Figure 11.

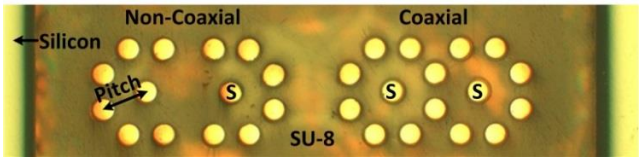


Figure 10. Fabricated polymer-enhanced coaxial vias and non-coaxial vias (for benchmarking).

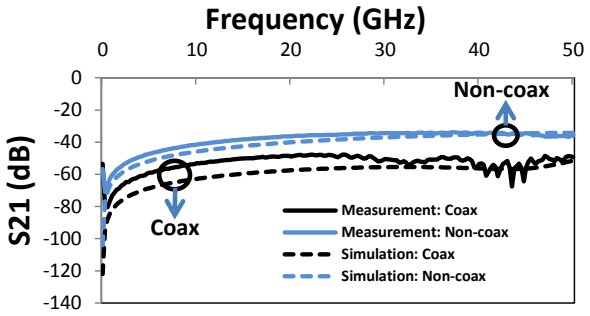


Figure 11. Coupling measurements of the fabricated polymer-enhanced coaxial and non-coaxial TSVs.

IV. Inductors: Fabrication and Characterization

Using the photodefined interposer technology, high-Q inductors are demonstrated over wells in thick silicon interposers. The proposed inductors can be fabricated in parallel to the polymer-enhanced TSVs enabling the fabrication of the envisioned silicon interposer system shown in Figure 1.

To fabricate the inductors, wells are etched in a silicon wafer followed by silicon nitride and titanium-copper deposition. Next, SU-8 filling, photodefinition, copper electroplating and CMP are performed in a similar fashion to the polymer-enhanced TSVs followed by fabrication of the electroplated inductors. Figure 12 illustrates the fabricated 1.5 and 2.5 turn inductors with 8-10 µm trace thickness, 55-65

µm trace width and 100 µm trace pitch over 1530 µm x 1030 µm wells in silicon. High-frequency measurements were performed for the fabricated inductors up to 50 GHz demonstrating a peak Q factor of 55 at 6.75 GHz with 1.14 nH inductance and a self-resonance frequency at 21 GHz for the 1.5 turn inductor, as shown in Figure 13.

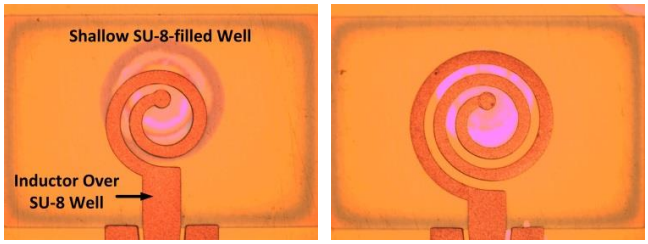


Figure 12. Fabricated inductors.

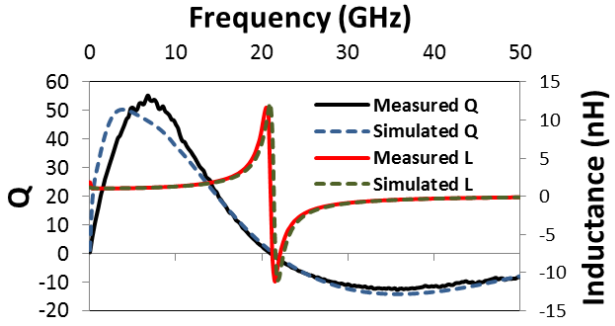


Figure 13. *Q* and *L* extraction using S11 measurements for 1.5 turn inductor [23].

V. Conclusions

This paper demonstrates a photodefined polymer-enhanced silicon interposer technology featuring high-performance polymer-enhanced TSVs and inductors. The proposed TSVs attain greater than 80% reduction in insertion loss at 50 GHz and 170 GHz compared to TSVs with silicon dioxide liners. Moreover, the coaxial configuration of the proposed TSVs is demonstrated with impedance-based design and shows a significant reduction in TSV coupling. Additionally, using the photodefined silicon interposer technology, high-Q (>50) inductors are demonstrated.

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References

1. L. A. Polka, "Package technology to address the memory bandwidth challenge for terascale computing," *Intel Technology Journal*, vol. 11, no. 03, Aug. 2007.
2. K. Kim "Silicon technologies and solutions for the data-driven world," in *Proc. IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 2015, pp. 8-13.
3. T. Dickson, Y. Liu, S. Rylov, B. Dang, C. Tsang, P. Andry, J. Bulzacchelli, H. Ainspan, X. Gu, L. Turlapati, M. Beakes, B. Parker, J. Knickerbocker, and D. Friedman, "An 8x10-Gb/s source synchronous I/O system based on high-density silicon carrier interconnects," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 4, pp. 884-896, Apr. 2012.
4. C. Erdmann, D. Lowney, A. Lynam, A. Keady, J. McGrath, E. Cullen, D. Breathnach, D. Keane, P. Lynch, M. De La Torre, R. De La Torre, P. Lim, A. Collins, B. Farley, and L. Madden, "A heterogeneous 3D-IC consisting of two 28 nm FPGA die and 32 reconfigurable high-performance data converters," *IEEE Journal of Solid-State Circuits,* vol. 50, no. 1, pp. 258-269, Jan. 2015.
5. W. Liao, C. Chiang, W. Wu, C. Fan, S. Chiu, C. Chiu, T. Chen, C. Hsieh, H. Chen, H. Lo, L. Huang, T. Wu, W. Chiou, S. Hou, S. Jeng, and Y. Doug, "A high-performance low-cost chip-on-wafer package with sub-µm pitch Cu RDL," in *Proc. IEEE 2014 Symposium on VLSI Technology (VLSI-Technology),* Honolulu, HI, USA, June 2014, pp. 1-2.
6. W. Lai, H. Chuang, C. Tsai, E. Yeh, C. Lin, T. Peng, L. Yen, W. Liao, J. Hung, C. Sheu, C. Yu, C. Wang, K. Yee, and D. Yu, "300mm size ultra-thin glass interposer technology and high-Q embedded helical inductor (EHI) for mobile application," in *Proc. IEEE International Electron Devices Meeting (IEDM),* Washington, DC, Dec. 2013, pp. 13.4.1-13.4.4.
7. L. Dussopt, Y. Lamy, S. Joblot, J. Lanteri, H. Salti, P. Bar, H. Sibuet, B. Reig, J.-F. Carpentier, C. Dehos, and P. Vincent, "Silicon interposer with integrated antenna array for millimeter-wave short-range communications," in *Proc. IEEE MTT-S International Microwave Symposium Digest (MTT)*, Montreal, QC, Canada, Jun. 2012, pp. 1-3.
8. W. Khan, C. Ulusoy, and J. Papapolymerou, "D-band characterization of co-planar wave guide and microstrip transmission lines on liquid crystal polymer," in *Proc. 63rd IEEE Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, May 2013, pp. 2304-2309.
9. I. Ndip, K. Zoschke, K. Lobbicke, M. Wolf, S. Guttowski, H. Reichl, K.-D. Lang, and H. Henke, "Analytical, numerical-, and measurement-based methods for extracting the electrical parameters of through silicon vias (TSVs)," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, no. 3, pp. 504-515, Mar. 2014.
10. V. Sundaram, Q. Chen, Y. Suzuki, G. Kumar, F. Liu, and R. Tummala, "Low-cost and low-loss 3D silicon interposer for high bandwidth logic-to-memory interconnections without TSV in the logic IC," in *Proc. 62nd IEEE Electronic Components and Technology Conference (ECTC)*, San Diego, CA, June 2012, pp. 292-297.
11. Q. Chen, C. Huang, D. Wu, Z. Tan, and Z. Wang, "Ultralow-capacitance through-silicon vias with annular air-gap insulation layers," *IEEE Transactions on Electron Devices*, vol. 60, no. 4, pp. 1421-1426, Apr. 2013.
12. D. Jung, H. Kim, S. Kim, J. Kim, B. Bae, J. Kim, J.-M. Yook, J.-C. Kim, and J. Kim, "30 Gbps high-speed characterization and channel performance of

coaxial through silicon via," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 11, pp. 814-816, Nov. 2014.
13. K. Oi, S. Otake, N. Shimizu, S. Watanabe, Y. Kunimoto, T. Kurihara, T. Koyama, M. Tanaka, L. Aryasomayajula, and Z. Kutlu, "Development of new 2.5D package with novel integrated organic interposer substrate with ultra-fine wiring and high density bumps," in *Proc. 64th IEEE Electronic Components and Technology Conference (ECTC),* Orlando, FL, May 2014, pp. 348-353.
14. Y. M. Khoo, T. G. Lim, S. W. Ho, R. Li, Y.-Z. Xiong, and X. Zhang, "Enhancement of silicon-based inductor Q-factor using polymer cavity," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 12, pp. 1973-1979, Dec. 2012.
15. S. Hu, Y.-Z. Xiong, L. Wang, R. Li, and T. G. Lim, "A millimeter-wave wideband high-gain antenna and its 3D system-in-package solution in a TSV-compatible technology," in *Proc. 64th IEEE Electronic Components and Technology Conference (ECTC),* Orlando, FL, May 2011, pp. 869-872.
16. V. Sukumaran, G. Kumar, K. Ramachandran, Y. Suzuki, K. Demir, Y. Sato, T. Seki, V. Sundaram, and R. R. Tummala, "Design, fabrication, and characterization of ultrathin 3-D glass interposers with through-package-vias at same pitch as TSVs in silicon," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, no. 5, pp. 786-795, May 2014.
17. J. Tong, Y. Sato, S. Takahashi, N. Imajyo, A. F. Peterson, V. Sundaram, and R. R. Tummala, "High-frequency characterization of through package vias formed by focused electrical-discharge in thin glass interposers," in *Proc. 64th IEEE Electronic Components and Technology Conference (ECTC),* Orlando, FL, May 2014, pp. 2271-2276.
18. R. Pierce, R. Islam, R. Henderson, and A. Blanchard, "SU-8 2000 millimeter wave material characterization," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 6, pp. 427-429, June 2014.
19. A. d. Campo and C. Greiner, "SU-8: a photoresist for high-aspect-ratio and 3D submicron lithography," *J. Micromechanics and Microengineering*, vol. 17, no. 6, pp. R81-R95, May 2007.
20. P. Thadesar and M. Bakir, "Novel photo-defined polymer-enhanced through-silicon vias for silicon interposers," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 7, pp. 1130-1137, July 2013.
21. H.-T. Yen, Y.-l. Lin, C. Hu, S. B. Jan, C.-C. Hsieh, M. F. Chen, C.-W. Kuo, H.-H. Chen, and M.-C. Jeng, "TSV RF de-embedding method and modeling for 3DIC," in *Proc. 23rd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, Saratoga Springs, NY, May 2012, pp. 394-397.
22. Z. Xu and J.-Q. Lu, "Through-silicon-via fabrication technologies, passives extraction, and electrical modeling for 3-D integration/packaging," *IEEE Transactions on Semiconductor Manufacturing*, vol. 26, no. 1, pp. 23-34, Feb. 2013.
23. R. L. Bunch, D. I. Sanderson, and S. Raman, "Quality factor and inductance in differential IC implementations," *IEEE Microwave Magazine*, vol. 3, no. 2, pp. 82-92, June 2002.